Andes Technology and Mirabilis Design Announce Collaboration on System-Level Models for Andes RISC-V Processor IP

Validated Architecture Models Enable Early Design Exploration and Pre-RTL Optimization

SANTA CLARA, CA, UNITED STATES, July 27, 2026 /EINPresswire.com/ -- Andes Technology, a leading supplier of high-performance, energy-efficient RISC-V processor IP and a Founding Premier Member of RISC-V International, and Mirabilis Design today announced a strategic collaboration to deliver system-level architecture models for Andes RISC-V processors. This partnership empowers SoC architects to evaluate and optimize processor-based designs well before RTL development.

> “Combining Andes RISC-V IP with VisualSim helps architects explore system trade-offs earlier and move into implementation with greater confidence.”
>
> *Vaishnavi Shankar, CEO, Mirabilis Design*

As part of this collaboration, Mirabilis Design has developed and validated system-level models for the Andes AX66 multicore and Andes A45 processors using the VisualSim® platform. The models allow architects to explore performance, power, and system behavior early in the design cycle, significantly reducing iteration time and architectural risk.

Parameterized Architecture Exploration Without Model Modification

The Andes system-level models support scalable multicore clusters, connected through AMBA AXI-based interconnects, with options for coherent cache hierarchies. Architectural exploration is performed entirely through parameter settings defined in the processor specifications, including:

- Number of cores per cluster and number of clusters
- Core configuration options
- Cache size, hierarchy levels, and coherency
- System address map and memory partitioning across multiple DRAMs

Users do not need to modify the model implementation. Design-space exploration is achieved by adjusting parameters, enabling rapid and repeatable evaluation of alternative configurations.

Software-Aware System Analysis

The models support execution of software traces and benchmarks, including workload distribution across multiple cores within a cluster. This capability allows architects to analyze their system-level performance impact early and align hardware configuration with software requirements.
This approach enables architects to tune processor topology, cache organization, and memory structure before RTL integration, improving predictability and reducing downstream design changes.

Industry Quotes

“Early architectural decisions are critical to achieving SoC optimal performance and efficiency,” said Dr. Charlie Su, President and CTO, Andes Technology. “This collaboration enables our customers to evaluate Andes RISC-V processor configurations at the system level and finalize specifications with greater confidence before implementation.”

“System-level modeling allows SoC architects to explore processor, cache, and memory trade-offs using real software behavior,” said Deepak Shankar, Founder, Mirabilis Design. “Our validated models of Andes AX66 and A45 processors support fast, parameter-driven exploration without requiring model rewrites.”

Availability and Roadmap

The Andes system-level processor models are available as part of the VisualSim® platform. Additional Andes RISC-V IP and configurations will be added over time to extend coverage across applications and markets.

About Mirabilis Design

Mirabilis Design provides system-level modeling and simulation solutions for early risk validation of semiconductors and electronic systems. VisualSim® enables architects to analyze power, performance, and functionality across complex SoC architectures.

About Andes Technology

As a Founding Premier member of RISC-V International and a leader in commercial CPU IP, Andes Technology (TWSE: 6533; SIN: US03420C2089; ISIN: US03420C1099) is driving the global adoption of RISC-V. Andes’ extensive RISC-V Processor IP portfolio spans from ultra-efficient 32-bit CPUs to high-performance 64-bit Out-of-Order multiprocessor coherent clusters. With advanced vector processing, DSP capabilities, the powerful Andes Automated Custom Extension (ACE) framework, end-to-end AI hardware/software stack, ISO 26262 certification with full compliance, and a

robust software ecosystem, Andes unlocks the full potential of RISC-V, empowering customers to accelerate innovation across AI, automotive, communications, consumer electronics, data centers, and mobile devices. Over 20 billion Andes-powered SoCs are driving innovations globally. Discover more at www.andestech.com and connect with Andes on LinkedIn, X (formerly Twitter) , YouTube and Bilibili.

Media Contact

Mirabilis Design Inc.
Kaveri Deepak
Marketing Intern
kaveri@mirabilisdesign.com

Andes Technology
Ruby Tseng
Deputy Manager Marketing Division
ruby670@andestech.com

Kaveri Deepak
Mirabilis Design
408-245-8992
email us here
Visit us on social media:
LinkedIn
Instagram
Facebook
YouTube
X
